|  | Application No.  | Applicant(s)  |
|--|--|---|
| Mada - CAU CUI   | 10/849,295   | CHEN ET AL.   |
| Notice of Allowability   | Examiner   | Art Unit  |
|  | José R. Díaz   | 2815  |
| The MAILING DATE of this communication appear All claims being allowable, PROSECUTION ON THE MERITS IS (herewith (or previously mailed), a Notice of Allowance (PTOL-85) NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGOT THE Office or upon petition by the applicant. See 37 CFR 1.313  | OR REMAINS) CLOSED in this apport or other appropriate communication GHTS. This application is subject to  | olication. If not included will be mailed in due course. THIS |
| 1. This communication is responsive to <u>2/2/05</u> .   |  |   |
| 2. X The allowed claim(s) is/are <u>1,3-13,15 and 18-23</u> .  |  |   |
| 3. $\boxtimes$ The drawings filed on <u>20 May 2004</u> are accepted by the Ex   | aminer.  |   |
| <ul> <li>4. Acknowledgment is made of a claim for foreign priority unally all b) Some* c) None of the:</li> <li>1. Certified copies of the priority documents have</li> <li>2. Certified copies of the priority documents have</li> <li>3. Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)).</li> <li>* Certified copies not received:</li> </ul> | been received. been received in Application No   |   |
| Applicant has THREE MONTHS FROM THE "MAILING DATE" of noted below. Failure to timely comply will result in ABANDONMI THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.  |  | complying with the requirements                               |
| 5. A SUBSTITUTE OATH OR DECLARATION must be submit INFORMAL PATENT APPLICATION (PTO-152) which give  |  |   |
| 6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must  (a) ☐ including changes required by the Notice of Draftsperso  1) ☐ hereto or 2) ☐ to Paper No./Mail Date  (b) ☐ including changes required by the attached Examiner's  Paper No./Mail Date  Identifying indicia such as the application number (see 37 CFR 1.8 each sheet. Replacement sheet(s) should be labeled as such in the             | on's Patent Drawing Review (PTO-<br>Amendment / Comment or in the O<br>84(c)) should be written on the drawin<br>te header according to 37 CFR 1.121(c | office action of ages in the front (not the back) of          |
| <ol> <li>DEPOSIT OF and/or INFORMATION about the depose attached Examiner's comment regarding REQUIREMENT F</li> </ol>   |  |   |
| Attachment(s)  |  |   |
| 1. Notice of References Cited (PTO-892)  | _  | atent Application (PTO-152)                                   |
| 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)   | 6. ☐ Interview Summary<br>Paper No./Mail Dat   |   |
| <ol> <li>Information Disclosure Statements (PTO-1449 or PTO/SB/08<br/>Paper No./Mail Date <u>5/20/04; 1/21/05</u></li> </ol>   |  |   |
| 4.   Examiner's Comment Regarding Requirement for Deposit  | 8. 🛛 Examiner's Stateme  | nt of Reasons for Allowance                                   |
| of Biological Material   | 9. 🗌 Other   |   |
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|  |  | PAY THOMAS<br>RY PATENT ÆXABATINER                            |
|  | 22. 2111001  |   |

U.S. Patent and Trademark Office PTOL-37 (Rev. 1-04)

## **EXAMINER'S AMENDMENT**

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Donald Featherstone (Reg. No. 33,876) on February 2, 2005.

Please amend claims 1, 3-5, 15 and 18, and cancel claims 2, 14, 16-17 and 24.

1. (Currently Amended) A one-time programming memory element capable of being manufactured in a 0.13  $\mu m$  or below CMOS technology, comprising:

a capacitor having an oxide layer capable of passing direct gate tunneling current;

a write circuit, including

a first switch coupled to said capacitor, <u>said first switch including a first</u> switch transistor connected between a first terminal of said capacitor and a first <u>voltage</u>, and

a second switch coupled to said <del>capacitor</del>; and <u>capacitor</u>, said <u>second</u>

<u>switch including a first switch transistor connected between a second terminal of said capacitor opposing said first terminal and a second voltage; and a read circuit coupled to said capacitor.</u>

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wherein said capacitor is one-time programmable as an anti-fuse by application of a program voltage across said oxide layer via said write circuit to cause direct gate tunneling current to rupture said oxide layer to form a conductive path having resistance of approximately hundreds of ohms or less.

## 2. (Cancelled)

- 3. (Currently amended) The one-time programming memory element of claim [[2]] 1, wherein each of said first and second switch transistors has an oxide layer thicker than said capacitor oxide layer.
- 4. (Currently amended) The one-time programming memory element of claim [[2]] 1, wherein said program voltage is equal to a difference between said first and second voltages.
- 5. (Currently amended) The one-time programming memory element of claim [[2]] 1, wherein said read circuit comprises plural read switch transistors coupled to said capacitor.
- 15. (Currently amended) A process, compatible with 0.13  $\mu m$  or below CMOS technology, for making a one-time programming memory element, comprising the steps of:

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forming a capacitor having an oxide layer capable of passing direct gate

tunneling current;

forming a write circuit, including the steps of

forming a first switch coupled to said the capacitor by connecting a first

switch transistor between a first terminal of the capacitor and a first voltage, and

forming a second switch coupled to said the capacitor by connecting a

second switch transistor between a second terminal of the capacitor opposing

the first terminal and a second voltage; and

forming a read circuit coupled to the capacitor,

wherein the capacitor is one-time programmable as an anti-fuse by application of

a program voltage across the oxide layer via the write circuit to cause direct gate

tunneling current to rupture the oxide layer to form a conductive path having resistance

of approximately hundreds of ohms or less.

14. (Cancelled)

16. (Cancelled)

17. (Cancelled)

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18. (Currently amended) The process of claim [[17]] 15, wherein each of the first

and second switch transistors are formed with an oxide layer thicker than the capacitor

oxide layer.

24. (Cancelled)

1. In addition to these changes, Applicant agreed to file a terminal declaimer to

overcome a provisional obviousness-type double patenting rejection over claim 20 of

copending Application 09/739,752.

2. The terminal disclaimer filed on February 2, 2005 disclaiming the terminal portion

of any patent granted on this application which would extend beyond the expiration date

of any patent granted on Application Number 09/739,752 has been reviewed and is

accepted. The terminal disclaimer has been recorded.

Reasons for Allowance

3. The following is an examiner's statement of reasons for allowance: the prior art

fails to teach, disclose, or suggest, either alone or in combination, a first write switch

transistor connected between a first terminal of said capacitor and a first voltage, and a

second write switch transistor connected between a second terminal of said capacitor

opposing said first terminal and a second voltage; wherein said capacitor is one-time

programmable as an anti-fuse.

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Any comments considered necessary by applicant must be submitted no later

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than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on

Statement of Reasons for Allowance."

Correspondence

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to José R. Díaz whose telephone number is (571) 272-

1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number

for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

TOMITHOMAS

SUPERVISORY PATENT EXAMINER

JRD 2/5/05